REMARKS

The present application is presently being appealed. In the final rejection, the Examiner noted informalities that are addressed here. In addition, Applicant found other informalities during preparation of the brief.

The Examiner notes that in claim 14, line 5, "a fifth p-channel" should be changed to --a sixth p-channel--. Applicant did not make this change because Applicant could not find any other fifth p-channel transistor. That being said, Applicant is not opposed to making the change if the Examiner still feels that it is appropriate.

In claim 23, the words "current path" erroneously appeared twice. This error has been corrected. With respect to the "third reference voltage" and the "first reference voltage," Applicant believes that the claim is correct as worded. Note that in claim 22, the first transistor is coupled to the third reference voltage and the second transistor is coupled to the first reference voltage. As a result, the third transistor is coupled between the first transistor and the third reference voltage and the fourth transistor is coupled between the second transistor and first reference voltage.

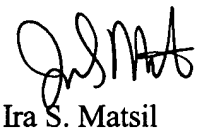
If the Examiner still believes that this claim (or any of the other claims) is incorrect, Applicant suggests that the Examiner speak with Applicant's attorney so that any remaining issues can be sorted out.

In addition, claim 7 has been amended to correct an obvious typographical error. Claim 2 has also been corrected to recite that the output pair is coupled to the fourth voltage level rather than the second voltage level. Applicant believes this claim is more consistent with claim 1.

In view of the above, Applicant respectfully submits that the formal issues have been resolved. If the Examiner has any questions or other correspondence regarding this application,

Applicant requests that the Examiner contact Applicant's agent at the below listed telephone number and address.

Respectfully submitted,



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Appendix I

Marked Version of Claims

2. (Twice Amended) The level shifting circuitry recited in claim 1, wherein the level-shifting circuitry includes:

an input transistor having a control electrode, a first electrode coupled to the input logic signal, and a second electrode;

a first switching transistor;

a second switching transistor;

an output pair of serially coupled complementary type transistors, a first one of the pair of transistors having a first electrode coupled to a source of the third voltage level through the first switching transistor and a control electrode coupled to the second electrode of the input transistor, a junction between the output pair of transistors providing the output terminal for the level-shifting circuitry, a control electrode of the second one of the pair of transistors being connected to the second electrode of the input transistor, the second one of the pair of transistors having a second electrode coupled to the [second] fourth voltage level through the second switching transistor; and

wherein the first and second switching transistors are fed by the enable/disable signal.

7. (Twice Amended) The level shifting circuitry recited in claim 2 and further comprising an additional transistor having a control electrode coupled to the junction, a [fist] first electrode coupled to the source of the third voltage level through the first switching transistor and a second electrode coupled to the second electrode of the input transistor.

23. (Amended) The circuit of claim 22 wherein the enable/disable section comprises:

a third transistor with a current path coupled in series the current path [current path] of the first transistor, the current path of the third transistor coupled between the third reference voltage node and the first transistor; and

a fourth transistor with a current path coupled in series the [current path] current path of the second transistor, the current path of the fourth transistor coupled between the first reference voltage node and the second transistor.